What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate in which a trench is formed;

a liner layer formed of a multi-layer of a silicon nitride layer and a silicon oxide layer on the sidewalls and bottom of the trench by atomic layer deposition; and

a buried insulating layer filled in the trench without a void.

2. The semiconductor device according to claim 1, further comprising:

a plurality of gate stack patterns formed on the semiconductor substrate on which the trench and the buried insulating layer are formed;

a plurality of gate spacers formed on the sidewalls of the gate stack patterns;

a first bubble prevention layer formed of a multi-layer of a silicon oxide layer and a silicon nitride layer on the gate spacers by atomic layer deposition; and

a first filling insulating layer filled without a void between the gate stack patterns on the first bubble prevention layer.

3. The semiconductor device according to claim 2, wherein the gate spacers are formed of a multi-layer of a silicon oxide layer and a silicon nitride layer by atomic layer deposition.

4. The semiconductor device according to claim 2, further comprising:

a plurality of bit line stack patterns formed on the first filling insulating layer;

a plurality of bit line spacers formed on the sidewalls of the bit line stack patterns;

a second bubble prevention layer formed of a multi-layer of a silicon oxide layer and a silicon nitride layer on the bit line spacers and on the bit line stack patterns by atomic layer deposition; and

a second filling insulating layer filled without a void between the bit line stack patterns on the second bubble prevention layer.

5. The semiconductor device according to claim 4, wherein the bit line spacers are formed of a multi-layer of a silicon oxide layer and a silicon nitride layer by atomic layer deposition.

6. The semiconductor device according to claim 1, wherein an oxide layer is formed by thermal oxidation or atomic layer deposition on the sidewalls and bottom of the trench before a liner layer is formed on the sidewalls and bottom of the trench.

7. The semiconductor device according to claim 2, wherein each gate stack pattern is formed by sequentially stacking a gate insulating layer, a first gate conductive layer, a second gate conductive layer, and a gate capping layer.

8. The semiconductor device according to claim 7, wherein the gate insulating layer is formed of a silicon oxide layer.

9. The semiconductor device according to claim 7, wherein the first gate conductive layer is formed of an impurity-doped polysilicon layer.

10. The semiconductor device according to claim 7, wherein the second gate conductive layer is formed of a metal silicide layer.

11. The semiconductor device according to claim 7, wherein the gate capping layer is formed of a silicon nitride layer.

12. The semiconductor device according to claim 4, wherein each bit line stack pattern is formed by sequentially stacking a barrier metal layer, a bit line conductive layer, and a bit line capping layer.

13. A semiconductor device comprising:

a semiconductor substrate in which a trench is formed;

a liner layer formed on the sidewalls and bottom of the trench;

a buried insulating layer filled in the trench;

a plurality of gate stack patterns formed on the semiconductor substrate;

a plurality of gate spacers formed on the sidewalls of the gate stack patterns;

a first bubble prevention layer formed of a multi-layer of a silicon oxide layer and a silicon nitride layer on the gate spacers and on the patterned gate stacks by atomic layer deposition;

a first filling insulating layer filled without a void between the gate stack patterns on the first bubble prevention layer;

a plurality of bit line stack patterns formed on the first filling insulating layer;

a plurality of bit line spacers formed on the sidewalls of the bit line stack patterns;

a second bubble prevention layer formed of a multi-layer of a silicon oxide layer and a silicon nitride layer on the bit line spacers and the bit line stack patterns by atomic layer deposition; and

a second filling insulating layer filled without a void between the bit line stack patterns on the second bubble prevention layer.

14. The semiconductor device according to claim 13, wherein the liner layer is formed of a multi-layer of a silicon nitride layer and a silicon oxide layer by atomic layer deposition, and the gate spacers and the bit line spacers are formed of a multi-layer of a silicon oxide layer and a silicon nitride layer by atomic layer deposition.

15. The semiconductor device according to claim 13, wherein an oxide layer is formed by thermal oxidation or atomic layer deposition on the sidewalls and bottom of the trench before a liner layer is formed on the sidewalls and bottom of the trench.

16. A method for fabricating a semiconductor device, the method comprising:

forming a trench to a depth in a semiconductor substrate;

forming a liner layer formed of a multi-layer of a silicon nitride layer and a silicon oxide layer on the sidewalls and bottom of the trench by atomic layer deposition; and

forming a buried insulating layer filled in the trench without a void.

17. The method for fabricating a semiconductor device according to claim 16, wherein the liner layer is formed without a vacuum break.

18. The method for fabricating a semiconductor device according to claim 16, wherein the silicon nitride layer forming the liner layer is formed using silicon source of silane (SiH_4), Si-alkyl, Si-halide, or Si-amide, and a nitrifying agent of ammonia, plasma ammonia, or plasma nitrogen.

19. The method for fabricating a semiconductor device according to claim 16, wherein the silicon oxide layer forming the liner layer is formed using silicon source of silane (SiH_4), Si-alkoxide, Si-alkyl, Si-halide, or Si-amide, and an oxidizing agent of water (H_2O), hydrogen peroxide, ozone, plasma O_2, N_2O, or plasma N_2O.

20. The method for fabricating a semiconductor device according to claim 16, wherein an oxide layer is formed by thermal oxidation or atomic layer deposition on the sidewalls and bottom of the trench before a liner layer is formed on the sidewalls and bottom of the trench.

21. The method for fabricating a semiconductor device according to claim 16, further comprising the steps of:

forming a plurality of gate stack patterns on the semiconductor substrate in which the trench and the buried insulating layer are formed;

forming a plurality of gate spacers on the sidewalls of the gate stack patterns;

forming a first bubble prevention layer of a multi-layer of a silicon oxide layer and a silicon nitride layer on the gate spacers and the gate stack patterns by atomic layer deposition; and

forming a first filling insulating layer without a void between the gate stack patterns on the first bubble prevention layer.

Sub A27

22. The method for fabricating a semiconductor device according to claim 21, wherein the gate spacers are formed of a multi-layer of a silicon oxide layer and a silicon nitride layer by atomic layer deposition.

Sub B1

23. The method for fabricating a semiconductor device according to claim 21, further comprising the steps of:

forming a plurality of bit line stack patterns on the first filling insulating layer;

forming a plurality of bit line spacers on the sidewalls of the bit line stack patterns;

forming a second bubble prevention layer of a multi-layer of a silicon oxide layer and a silicon nitride layer on the bit line spacers and the bit line stack patterns by atomic layer deposition; and

forming a second filling insulating layer without a void between the bit line stack patterns on the second bubble prevention layer.

24. The method for fabricating a semiconductor device according to claim 22, wherein the second bubble prevention layer is formed without a vacuum break.

25. The method for fabricating a semiconductor device according to claim 22, wherein the bit line spacers are formed of a multi-layer of a silicon nitride layer and a silicon oxide layer by atomic layer deposition.

26. The method for fabricating a semiconductor device according to claim 20, wherein each gate stack pattern is formed by sequentially stacking a gate insulating layer, a first gate conductive layer, a second gate conductive layer, and a gate capping layer.

27. The method for fabricating a semiconductor device according to claim 26, wherein the gate insulating layer is formed of a silicon oxide layer.

28. The method for fabricating a semiconductor device according to claim 26, wherein the first gate conductive layer is formed of an impurity-doped polysilicon layer.

29. The method for fabricating a semiconductor device according to claim 26, wherein the second gate conductive layer is formed of a metal silicide layer.

30. The method for fabricating a semiconductor device according to claim 26, wherein the gate capping layer is formed of a silicon nitride layer.

31. The method for fabricating a semiconductor device according to claim 22, wherein each bit line stack pattern is formed by sequentially stacking a barrier metal layer, a bit line conductive layer, and a bit line capping layer.

32. A method for fabricating a semiconductor device, the method comprising the steps of:

forming a trench on a semiconductor substrate with a predetermined depth;

forming a liner layer of a multi-layer of a silicon nitride layer and a silicon oxide layer on the sidewalls and bottom of the trench by atomic layer deposition;

forming a buried insulating layer filled in the trench without a void;

forming a plurality of gate stack patterns on the semiconductor substrate on which the trench and the buried insulating layer are formed;

forming a plurality of gate spacers on the sidewalls of the gate stack patterns;

forming a first bubble prevention layer of a multi-layer of a silicon oxide layer and a silicon nitride layer on the gate spacers and the gate stack patterns by atomic layer deposition;

forming a first filling insulating layer without a void between the gate stack patterns on the first bubble prevention layer;

forming a plurality of bit line stack patterns on the first filling insulating layer;

forming a plurality of bit line spacers on the sidewalls of the bit line stack patterns;

forming a second bubble prevention layer of a multi-layer of a silicon oxide layer and a silicon nitride layer on the bit line spacers and the bit line stack patterns by atomic layer deposition; and

forming a second filling insulating layer without a void between the bit line stack patterns on the second bubble prevention layer.

33. The method for fabricating a semiconductor device according to claim 32, wherein the liner layer is formed of a multi-layer of a silicon nitride layer and a silicon oxide layer by atomic layer deposition, and the gate spacers and the bit line spacers are formed of a multi-layer of a silicon oxide layer and a silicon nitride layer by atomic layer deposition.

34. The method for fabricating a semiconductor device according to claim 32, wherein the liner layer, the gate spacers, the first bubble prevention layer, the bit line spacers, or the second bubble prevention layer are formed without a vacuum break.

35. The method for fabricating a semiconductor device according to claim 32, wherein an oxide layer is formed by thermal oxidation or atomic layer deposition on the sidewalls and bottom of the trench before a liner layer is formed on the sidewalls and bottom of the trench.